IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		TI-33763
	Song Wu, et al.	Art Unit: 2611
Serial No:	10/603,302	Examiner: Jaison Joseph
Filed:	June 25, 2003	Conf. No.: 5280
For:	Decision Feedback Equalization for High Speed Serial Links	

Appeal Brief Under 37 C.F.R. §41.37

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §41.37 in connection with the above-identified application in response to the Final Rejection mailed May 15, 2008, and the Notice of Appeal mailed by Applicant on October 10, 2008.

Real Party in Interest

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 013275 and frame 0196 to 0198.

Related Appeals and Interferences

There are no appeals of interferences related to this appeal in this application.

Status of the Claims

Claims 1, 2, 4, and 6-12 are the subject of this appeal. Claims 1, 2, 4, and 6-12 are rejected. Claims 3, 5, and 13-25 have been canceled. This application was filed on June 25, 2003.

Status of Amendments Filed After Final Rejection

The Appellants filed an amendment under 37 C.F.R. § 1.116 on August 1, 2008 in response to the Office Action dated May 15, 2008, with no amendments to the claims.

Summary of Claimed Subject Matter

Specification page 11, line 3 to page 12, line 8, and Figure 1 provide a concise explanation of the invention defined in claim 1.

The input for receiving from a communication transmitter apparatus an input analog communication signal in claim 1 is the input to the AGC in Figure 1.

The feedforward equalizer in claim 1 is summation node 15 in Figure 1.

The sampler in claim 1 is sampler 13 in Figure 1.

The feedback equalizer in claim 1 includes the analog-to-digital converters DAC in Figure 1.

Shown in FIGURE 1, an analog AGC (automatic gain control) block buffers the analog input to prevent the feedback signal $s(t)$ from echoing back to the line. The buffered analog

input signal $y(t)$, in this example current, is wire summed with the synthesized signal $s(t)$. The sampling receiver 13 takes samples from the mixed signal $z(t)$ to make the symbol decision. The decision symbols are then fed back to construct the new feedback signal $s(t)$. As shown in FIGURE 1, the decision symbols S_k (k = 1, … K) at different delay stages drive respective current source digital to analog converters (DAC) which are controlled by weights dfe_k (k = 1, … K) that define the taps of feedback signal $s(t)$.

In some embodiments, the tap weights dfe_k are real numbers in 2's complement format. Assuming, for example, that each weight dfe_k includes B bits which represent the magnitude of dfe_k, plus an additional bit to represent the sign of dfe_k, then for each of the K taps, the associated DAC has B parallel-connected current switch transistors. In some embodiments of FIGURE 1A, the B magnitude bits of dfe_k are thermometer-coded, and each of the resulting B thermometer-coded bits controls a respectively corresponding one of the B transistor switches. Each decision symbol S_k includes complementary bits s_k and $\overline{s_k}$ which are combined (e.g. multiplied) with the associated sign bit as shown in FIGURE 1A to control the polarity of the current that the corresponding DAC contributes to the wire summation node 15. Node 15 thus functions as a feedforward equalizer.

The receiver sampler and each delay stage are triggered by the symbol clock (not explicitly shown), so the $s(t)$ waveform is a square wave with each pulse having one-symbol duration T. The leading tap is time critical, so some embodiments require the circuit delay from the decision sampler 13 to the leading tap DAC output to be less than half of the symbol period.

Grounds for Rejection to be Reviewed on Appeal

Whether claims 1, 2, 4, 6-9, 11, and 12 are unpatentable under 35 USC 103(a) over U.S. Patent Application Publication No. 2003/0058930 and U.S. Patent No. 6,469,988.

Whether claim 10 is unpatentable under 35 USC 103(a) over U.S. Patent Application Publication No. 2003/0058930, U.S. Patent No. 6,469,988, and U.S. Patent No. 7,027,499.

Arguments

Rejection under 35 USC 103(a) over U.S. Patent Application Publication No. 2003/0058930 and U.S. Patent No. 6,469,988

Claims 1, 2, 4, 6-9, 11, and 12

Claim 1 includes "... said digital-to-analog conversion portion includes a plurality of digital-to-analog converters … having respective outputs coupled to said feedforward equalizer...". U.S. Patent Application Publication No. 2003/0058930 and U.S. Patent No. 6,469,988 do not show, teach, or suggest the above recited limitations of claim 1. U.S. Patent Application Publication No. 2003/0058930 and U.S. Patent No. 6,469,988 do not teach how the plurality of digital to analog converters (DACs) in U.S. Patent No. 6,469,988 would be substituted into the device of U.S. Patent Application Publication No. 2003/0058930 to obtain the device of claim 1. In U.S. Patent No. 6,469,988, the DACs are used as tail current sources for respective differential pair stages. The outputs of each DAC in U.S. Patent No. 6,469,988 are not coupled to a single device such as a feed forward equalizer of claim 1.

Rejection under 35 USC 103(a) over U.S. Patent Application Publication No. 2003/0058930, U.S. Patent No. 6,469,988, and U.S. Patent No. 7,027,499

Claim 10

Claim 10 depends from claim 1. Claim 1 includes "... said digital-to-analog conversion portion includes a plurality of digital-to-analog converters … having respective outputs coupled to said feedforward equalizer...". U.S. Patent Application Publication No. 2003/0058930, U.S. Patent No. 6,469,988, and U.S. Patent No. 7,027,499 do not show, teach, or suggest the above recited limitations of claim 1. U.S. Patent Application Publication No. 2003/0058930, U.S. Patent No. 6,469,988, and U.S. Patent No. 7,027,499 do not teach how the plurality of digital to analog converters (DACs) in U.S. Patent No. 6,469,988 would be substituted into the device of U.S. Patent Application Publication No. 2003/0058930 to obtain the device of claim 1. In U.S. Patent No. 6,469,988, the DACs are used as tail current sources for respective differential pair stages. The outputs of each DAC in U.S. Patent No. 6,469,988 are not coupled to a single device such as a feed forward equalizer of claim 1.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1, 2, 4, and 6-12 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

To the extent necessary, the Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 20-0668 of Texas Instruments Inc.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

/Alan K. Stewart/
Alan K. Stewart
Attorney for Applicant
Reg. No. 35,373

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
Phone: 972-917-5466
Fax: 972-917-4418

CLAIMS APPENDIX

1. A communication receiver apparatus, comprising:

an input for receiving from a communication transmitter apparatus an input analog communication signal;

a feedforward equalizer coupled to said input for producing in response to said input analog communication signal an equalized analog communication signal;

a sampler coupled to said feedforward equalizer for producing digital communication information in response to said equalized analog communication signal;

a feedback equalizer coupled between said sampler and said feedforward equalizer for controlling said feedforward equalizer in response to said digital communication information;

wherein said feedback equalizer includes a digital-to-analog conversion portion having an input coupled to said sampler for receiving said digital communication information, said digital-to-analog conversion portion having an output coupled to said feedforward equalizer;

wherein said digital-to-analog conversion portion includes a plurality of digital-to-analog converters having respective inputs coupled to said sampler and having respective outputs coupled to said feedforward equalizer.

2. The apparatus of Claim 1, wherein said feedforward equalizer includes a wire summation node.

4. The apparatus of Claim 1, wherein said feedforward equalizer includes a wire summation node.

6. The apparatus of Claim 1, wherein each of said digital-to-analog converters includes a current source digital-to-analog converter.

7. The apparatus of Claim 6, wherein said outputs of said digital-to-analog converters are connected together at an input of said feedforward equalizer.

8. The apparatus of Claim 1, wherein said feedforward equalizer includes a wire summation node.

9. The apparatus of Claim 1, wherein said feedback equalizer includes a delay apparatus coupled between said sampler and said digital-to-analog converters for providing said digital communication information to said digital-to-analog converters at respectively different points in time.

10. The apparatus of Claim 1, wherein said input analog communication signal carries a SONET communication.

11. The apparatus of Claim 1, wherein said feedback equalizer includes a control input for receiving first control information, said feedback equalizer responsive to said control information for controlling said feedforward equalizer, said control information designed to minimize interference at temporal boundaries between data symbols carried by said equalized analog communication signal.

12. The apparatus of Claim 11, wherein said input analog communication signal is produced by the communication transmitter apparatus in response to second control information, said first control information designed in conjunction with the second control information to minimize interference at points in time between said temporal boundaries.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None